DAVID L. OSTER

Santa Barbara, CA 93105

www.daveoster.com
dave@daveoster.com

Experienced, innovative engineer seeking employment or contract-based system architecture and design opportunities in digital or embedded systems. Experience includes architectural development and design team management of embedded and digital systems, large system interfaces, and digital communication systems. Adept in CAD and logic design environments. Working knowledge of programming.

PROFESSIONAL SKILLS

- Project inception, execution and leadership
- FPGA, CPLD with VHDL
- Embedded system design
- Project planning, system architecture
- ANSII C, assembly language
- Embedded power management
- CAD/CAE using PCAD, Altium, Protel, PADS

WORK EXPERIENCE

Digital Subsystem Design and Integration:

Consulting Digital System Engineer, 2008-2012 **FLIR, Commercial Sys., Santa Barbara, CA**
Updated VHDL processing modules for real-time frame processing in IR cameras. Implemented new real-time image processing algorithms for IR cameras under direction of specialist. Tested and validated low noise power and DAC ASIC, which required design of a test platform including a 40dB amplifier to measure noise and an FPGA based DDA type pattern generator for video DAC testing.

Consulting Digital System Engineer, 2007 **Truevision, Santa Barbara, CA**
Debugged CameraLink problems in video system. Design oversight and study of video system control FPGA, a Spartan 3 part. Real-time picture processing functions added to design after initial checkout and integration.

Consulting Digital System Engineer, 2007 **Sensus Metering Systems, Goleta, CA**
Debugged and eliminated electric field noise in power supply design of utility meter transponder (included PCB CAD). Identified and resolved audible noise in Zigbee transponder caused by LDO instability.

Consulting Digital System Engineer, 2006 **Vareda Engineering, Goleta, CA**
Co-designed video test system. Defined system interface to microprocessor. Defined and implemented overall digital architecture and operation using multiple FPGAs. Implementation used Xilinx with hierarchical VHDL, procedures (for maintainability), and IP macros. Timing simulation utilized the ISE simulator package. Also designed power sequencing, management, and control. See www.vareda.com.

Consulting Digital System Engineer, 2004-2005 **Sensus Metering Systems, Goleta, CA**
Designed PCMCIA-based microprocessor subsystem for semi-automated data collection from wireless utility meters. Initial design used PCMCIA interface with required configuration structures for system software. Final design included multiple 8-bit microprocessors, an FPGA (Spartan III), and a low power 900MHz wireless transceiver, and an interface to a higher power direct digital spread spectrum transceiver. Xilinx FPGA VHDL code was multilevel using procedures for maintainability and incorporated the DSP logic needed to receive and decode the DDSS signal. Simulation used Modelsim. Additional tasks included test and qualification of boost power source circuits for severe environment, low power application (meter transponder).

Embedded Systems:

Consulting Engineer, 2012-2013 **FLIR, Electro-Optical Components Division, Ventura, CA**
Designed and debugged multiple Microchip PIC18F based controllers for SWIR lasers and photodiode detectors. System control was via the PIC UART port. Code was written in CCS C. Laser drivers were current controlled with thermal feedback and compensation and/or photodiode feedback. PIC capture and compare timer facilities were utilized and in some cases, clock switching and power domain switching were employed for power conservation. Multiple point-of-use switching regulators were load and line step simulated for stability and performance. Advised other engineers on power control issues, point of use regulators.

Consulting Engineer, 2008-2012 FLIR, Commercial Systems Division, Santa Barbara, CA
Debugged and stabilized buck current fed push pull power supply for IR camera system. Tested, validated, and corrected problems with embedded power supply ASIC. Designed standards based surge protection for devices subject to induced lightning surges (EN61000-4-5 and EN50130-4). Debugged and tuned system level switching power supply for M-series IR cameras. Analyzed induced lightning surge protection on IR cameras. Built low voltage surge generator to validate and test surge components and surge protected systems. Redesigned surge protection for Foveus and Pelagic cameras. Performed subjective visible image noise sensitivity analysis from noise injected into Tau IR camera power regulator outputs and design software to interpolate and weight the spectral output. Designed Ethernet activated current limited power switch for Voyager 3 maritime camera. Debugged radiated emissions susceptibility problem with motion control position sensors on M-series camera. Created a simple radiated emissions test system for further test and troubleshooting of M-series with servo stabilizer. Refined bench top surge generator and test setup for use troubleshooting Traffic Cam product video path surge circuitry. Redesigned and tested IP Bullet power supply frontend and surge limiting circuitry. Designed isolated, battery powered surge peak voltage indicator for surge circuitry debugging. Participated in design and debugging of low cost maritime IR camera using POE for power and with opto isolated video output.

Consulting Engineer, 2008-2009 Sensus Metering Systems, Goleta, CA
Designed embedded power supply system for handheld battery powered instrument used for remote utility setup. Tested design over temperature and load range. Designed changes to a magnetically coupled communication system for two different instruments. Changes required analysis of magnetic field shape, strength, and permeability to make coupling to target device easier by requiring less precision in physical placement.

Embedded System Hardware Engr., 2007-2008 Robert Ramey Consulting, Santa Barbara, CA
Designed circuit and PCB for a USB based PIC microcontroller system used in a one handed chording keyboard for disabled persons or graphic artists. PCB was designed to be used for left and right hand versions.

Digital System Designer/Consultant, 2002-2004 Sonos, Santa Barbara, CA
Responsible for microprocessor, audio subsystem, power supply, and network hub design and development. Worked with product manager to define requirements with low production cost and desired consumer features. Developed BOM, managed prototype efforts, and performed testing.

Embedded System Consultant, 2001-2003 Machine Talker, Santa Barbara, CA
Responsible for development of hardware and design of ad-hoc, partial-mesh wireless network data protocol for low power 900MHz ISM intelligent nodes. Used Atmel ATmega128 processor with multichannel 12-bit analog subsystem, accelerometers, temperature sensors, and humidity sensors with TI TRF6901 ISM transceiver. Battery management was built into protocol and power system. Worked with BlueTooth and considered the proposed IEEE 802.15.4 pan as alternative network platforms.

Director, Hardware Engineering, 1996-2001 Connected Systems, Santa Barbara, CA
Responsible for system architecture and overall design for PC type embedded systems with DSP coprocessor used for Computer Telephony Interface (CTI) applications such as voicemail. Issues addressed included power conversion, regulation, and low-power battery backup, packaging and overall logic and system design. Agency approvals such as FCC part 15, part 68, and UL1950B domestically, and CTR21, CE, and TUV internationally were required to bring system-level products to market. Used VHDL, AHDL, and CUPL for logic design. Managed two additional hardware designers. Interfaced with test labs and agencies needed for telephony, emissions, and safety approvals.

Consulting Design Engineer, 1980 Digital Sound, Santa Barbara, CA
Designed an interface between a 16-bit analog subsystem and a Varian 620i minicomputer.

Design Engineer, 1979-1980 Digital Image Systems, Santa Barbara, CA
Designed a Z-80 based video frame-grabber imaging system for commercial and entertainment use. A complete user interface and operating monitor were written in macro assembly as part of the job. Images were enhanced and dithered for dot-matrix printing. The same microprocessor imaging system was later used as a controller for a computer controlled 3-D router/shaper system. A FIFO based 5 ¼" floppy system was added for picture storage.

Digital Communication Subsystems:

CEO, 1990-1996 MultiAccess Computing, Santa Barbara, CA

Responsible for concept, hardware architecture and design, software behavior and overall design of several adapter and system level products for wide area networking based on SMDS and frame relay technologies as well as related 56k, T1/FT1, and T3 carrier interfacing. Participated in defining the IEEE 802.6 DQDB standard on which SMDS and connectionless ATM are based. Managed eight engineers and technicians.

VP Hardware Engineering, 1981-1990 Communication Machinery Corp, Santa Barbara, CA
Principal architect and designer for the CMC series of system bus based Ethernet LAN cards utilizing the MC68000 processor and DRAM for code and data, onboard BIST and link level and driver network control code. Also designed discrete emulator for AMD Ethernet chip, Multibus I to ARPAnet interface, and an FDDI adapter for the SUN 9U backplane.

Consulting Design Engineer, 1980 Channel Systems Int'l, Santa Barbara, CA
Designed Z-80 based communications subsystem for IBM Series 1 minicomputer. Developed custom Fortran application for netlist generation.

Design Engineer, 1975-1979 ACC, Santa Barbara, CA
Designed a variety of mainframe, network, and PDP-11 system interfaces for the emerging ARPAnet using TTL, PROM based state machines, and microprocessor technology. Designs include several BBN-1822 IMP to mainframe and PDP-11 interfaces, an SDLC based Error Control Unit to extend the range of the BBN-1822, and a Z-80 based embedded communication controller for the PDP-11 and VAX. Wrote diagnostic code for hardware in macro-11.

Design Engineer, 1970-1975 Speech Communications Research Lab, Santa Barbara, CA
Provided computer system support and engineering in form of maintenance repair, drivers and software modules, and hardware upgrades. Kept the PDP-8 and PDP-11s operational. Designed software on spec. Hardware designs include microcoded variable precision floating point hardware for the PDP-11, an analog subsystem for the PDP-11, and a multi-terminal multiplexed coaxial bus for an early ARPAnet terminal server.

PATENTS

Patent #7154381
System and method for operating a sensed power device over data wiring
Issued 12/26/06

EDUCATION

Bachelor of Science in Electrical Engineering (BSEE), 1970
University of California, Santa Barbara, CA

Supplementary courses in programming and math, 2005-2006
Santa Barbara City College, Santa Barbara, CA

REFERENCES

References and detailed contact information available on request.